

UNITED STATES PATENT APPLICATION  
FOR  
SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME

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Field of the Invention:

[001] The invention generally relates to a semiconductor device and method of forming the same, and more particularly to a device and method that improves operating characteristics by forming a transistor in upper silicon of a SOI (silicon-on-insulator) wafer, that is, in an active region of a second silicon layer, wherein a silicide layer is formed at an interface of the active region and a device isolation region.

Description of the Prior Art:

[002] As the length of a gate electrode of a semiconductor device is reduced to below 0.15  $\mu\text{m}$ , the channel resistance of the device is reduced, which relatively increases the importance of the parasitic resistance during device operation. Due to this phenomenon, salicide technology is required to reduce contact resistance between a gate and a diffusion layer in a high speed logic device.

[003] In addition, because increasing the integration level of a device requires increasing wiring using a diffusion layer, reduction in the resistance of the diffusion layer and the gate electrode is required. However, the diffusion layer becomes shallower due to a decrease in the width of the gate electrode. Thus, the thickness of salicide is reduced, which undesirably increases the resistance of the diffusion layer.

[004] Accordingly it is desirable to lower the resistance of the diffusion layer while solving the problem of a shallow junction using a SOI wafer in highly integrated semiconductor devices.

[005] One solution is to use cobalt salicide, which has no dependency on the line width. However, this may result in leakage current. Leakage current is

generated by lateral growth of silicide during formation of thick silicide in a depletion region at the edge of the field oxide and by diffusion of high melting metal used as silicide during the process of forming thick silicide.

### SUMMARY OF THE INVENTION

[006] The present invention provides a semiconductor device and method of forming the same that allows high integration of the device by forming a silicide layer at the interface of a device isolation film, which defines an active region in a second silicon layer of a SOI wafer and a second silicon layer of the active region.

[007] The present invention provides a semiconductor device comprising a SOI wafer having a stacked structure of a first silicon layer, a buried insulating film and a second silicon layer; a trench formed by removing a predetermined region of the second silicon layer; a first silicide layer formed at the side walls of the trench; a device isolation film defining an active region of the SOI wafer formed by filling the trench; a gate electrode having a gate insulation film formed on the active region of the SOI wafer; an insulation spacer formed at the side walls of the gate electrode; impurity junction regions formed at both sides of the gate electrode in the active region of the SOI wafer; and a second silicide layer formed on the gate electrode and the impurity regions, wherein the first and the second silicide layers are comprised of a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten.

[008] The present invention also provides a method of forming a semiconductor device comprising forming a pad insulating film on a SOI wafer having a stacked structure of a first silicon layer, a buried insulating film, and a second silicon layer; etching a predetermined region of the pad insulating film and

the second silicon layer by a lithography process using a device isolation mask to form a trench exposing the buried insulating film; forming a first silicide layer at side walls of the trench; forming a device isolation film defining an active region by filling the trench; forming a transistor having a gate electrode, a insulation spacer and impurity junction regions on the second silicon layer in the active region; and forming a second silicide layer on the gate electrode and the impurity junction regions.

[009] A first silicide layer is formed by forming a high melting point metal layer on the entire surface having a thickness in a range of 100 – 300Å using a CVD method, performing an annealing process, and removing an unreacted portion of the high melting point metal layer, wherein the high melting point metal layer comprises a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten. The annealing process is performed at a temperature in a range of 900 – 1000 °C for 10 – 60 seconds, and the unreacted portion of the high melting point metal layer is removed by performing a first wet etch process using a HNO<sub>3</sub> solution and a second wet etch process using a HF solution diluted in the HNO<sub>3</sub> solution. A second silicide layer is formed by forming a high melting point metal layer having a predetermined thickness on the entire surface, performing a first annealing process at a temperature in a range of 650 – 750 °C for 10 – 30 seconds, removing an unreacted portion of the high melting point metal layer, and performing a second annealing process at a temperature in a range of 800 – 1000 °C for 10 – 30 seconds, wherein the high melting point metal layer comprises a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten.

[010] In accordance with the present invention, a transistor having an improved operating characteristics sufficient for high integration is provided by etching a second silicon layer of a SOI wafer to form a trench exposing a buried oxide film, forming a device isolation film filling the trench, wherein a silicide layer is formed at the side walls of the trench before filling the trench, thereby forming a silicide layer at the interface between a device isolation film in a device isolation region and a second silicon layer in an active region, and forming the transistor in the second silicon layer by subsequently using a salicide process.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

[011] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[012] Figs. 1a – 1e are cross-sectional views illustrating a semiconductor device and method of forming the same according to an embodiment of the present invention.

#### **DETAILED DESCRIPTION**

[013] The present invention will be described in detail by way of an embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

[014] Figs. 1a – 1e are cross-sectional views illustrating a semiconductor device and a method of forming the same according to an embodiment of the present invention.

[015] The device shown in Fig. 1a may be formed as follows. A SOI wafer comprising a first silicon layer 11, a buried oxide film 13, and a second silicon layer

15 is formed. A pad nitride film 17 is then formed on the SOI wafer. Next, pad nitride film 17 and second silicon layer 15 are etched by a photolithography process using a device isolation mask (not shown) to form a trench 50 exposing buried oxide film 13. Thereafter, a high melting point metal layer 19 with predetermined thickness is formed on the entire surface. High melting point metal layer 19 may be formed of tungsten having a thickness in a range of 100 – 300 Å using a CVD method. Nickel, cobalt, or titanium may be used instead of tungsten to form the high melting point metal layer 19.

[016] Referring now to Fig. 1b, the SOI wafer is annealed to silicidize high melting point metal layer 19 of Fig. 1a contacting the second silicon layer 15, thereby forming a first silicide layer 21 at the sidewall of trench 50. At this time, the annealing process is preferably performed at a temperature in a range of 900 – 1000 °C for 10 – 60 seconds.

[017] Next, the high melting point metal layer 19 of Fig. 1a formed on the buried oxide film 13 and pad nitride film 17 is removed by a wet etch method. At this time, the wet etch method includes a first wet etch process using HNO<sub>3</sub> solution and a second wet etch process using HF solution diluted in the HNO<sub>3</sub> solution.

[018] Referring now to Fig. 1c, an insulating film for device isolation film filling trench 50 is formed on the entire surface and then planarized to form a device isolation film 23 filling trench 50 of Fig. 1a. A first silicide layer 21 is then provided at the interface of device isolation film 23 and second silicon layer 15.

[019] Referring now to Fig. 1d, a thermal oxide film (not shown) and a conductive layer (not shown) for a gate electrode are deposited on the entire surface

including second silicon layer 15. They are then patterned by a lithography etch process using a gate electrode mask (not shown) to form a gate electrode 27 having a gate oxide film 25 at the interface of second silicon layer 15. Also, low concentration impurities are injected into second silicon layer 15 using gate electrode 27 as a mask to form a low concentration impurity junction region 29.

[020] Next, an insulating film spacer 31 is formed at the sidewall of gate electrode 27. Then, high concentration impurities are injected into the second silicon layer 15 using the insulating film spacer 31 and the gate electrode 27 as a mask to form a high concentration impurity junction region 33.

[021] With reference to Fig. 1e, a second silicide layer 35 is formed on impurity high concentration junction region 33 and gate electrode 27 using a salicide process, thereby reducing the resistance of the impurity junction region 33 and improving the operating characteristic of the device. In one embodiment, the salicide process comprises forming a high melting point metal with a predetermined thickness on the entire surface where gate electrode 27 and impurity high concentration junction region 33 are formed, performing a first annealing process at a temperature in a range of 650 – 750 °C for 10 – 30 seconds, removing non-reacted high melting point metal, and performing a second annealing process at a temperature in a range of 800 – 1000 °C for 10 – 30 seconds to form a silicide layer.

[022] As described above, a semiconductor device and method of forming the same according to the present invention provides a transistor using a SOI wafer, wherein a silicide layer is formed on and at the sidewall of the impurity high concentration junction region, which minimizes the resistance of an impurity junction

region and improves operating characteristics of the semiconductor device.

Further, the present invention provides a high-speed semiconductor device without using a high cost lithography process, thus reducing the manufacturing cost of the semiconductor device.

[023] The present invention has been described with reference to particular embodiments in connection with particular applications. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

[024] It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.

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